

**POWER REGULATION LOOP PERFORMS TWO FUNCTIONS**

**Field of the Invention**

The present invention relates to electronic circuits and, more particularly,  
5 to electronic circuits for power regulation.

**Background**

In the electronics industry, there is a need for regulating current. Many  
battery powered electronic devices include components for monitoring the current to  
and from a load, such as a battery pack. This is typically done by putting a sense  
10 resistor in the path between the battery pack and the load and also between the charging  
unit and the battery pack. A regulating circuit then measures the voltage across the  
sense resistors and limits the current to or from the battery pack accordingly. This  
limiting is typically performed by using a transistor in the current path from the battery  
pack to the load or charging unit and by causing the transistor's control terminal to be  
15 driven in response to the voltage across the sense resistor.

A transistor exhibits low resistance when its control terminal is held at a  
voltage appropriate to turn the transistor "full on." In current regulating circuitry, this is  
often accomplished through the use of an amplifier coupled to the sense resistor with  
the amplifier output driving the control terminal of the transistor. With the appropriate  
20 choice of sense resistor and amplifier characteristics, the current regulating circuitry can  
be constructed such that for currents less than a regulation current limit, the amplifier  
drives the control terminal of the transistor to a full on state. As current through the  
sense resistor increases above the regulation current limit, the amplifier drives the  
control terminal of the transistor to reduce the current to the regulation current limit.  
25 This has the effect of providing little resistance when current passing through the  
regulating circuitry is less than the regulation current limit and provides the appropriate  
amount of resistance through the transistor to limit the current to the regulation current  
when a load tries to draw an excess amount of current.

### **Brief Description of the Drawings**

FIGURE 1 shows a circuit for a power regulation loop that operates in two modes using a single comparator;

FIGURE 2 illustrates a circuit for a power regulation loop arranged to  
5 operate in linear control mode; and

FIGURE 3 illustrates a process for a power regulation loop that performs two functions, in accordance with aspects of the invention.

### **Detailed Description**

In the following detailed description of exemplary embodiments of the  
10 invention, reference is made to the accompanied drawings, which form a part hereof, and which is shown by way of illustration, specific exemplary embodiments of which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and other changes may be made, without departing  
15 from the spirit or scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims.

Throughout the specification and claims, the following terms take the meanings explicitly associated herein, unless the context clearly dictates otherwise. The  
20 meaning of "a," "an," and "the" includes plural reference, the meaning of "in" includes "in" and "on." The term "connected" means a direct electrical connection between the items connected, without any intermediate devices. The term "coupled" means a direct electrical connection between the items connected, or an indirect connection through one or more passive or active intermediary devices. The term "circuit" means either a  
25 single component or a multiplicity of components, either active and/or passive, that are coupled to provide a desired function. The term "signal" means at least one current signal, voltage signal, electromagnetic wave signal, or data signal. The term "battery" includes single cell batteries and multiple cell batteries. The term "cell" includes single

rechargeable cells and multiple rechargeable cells. The term "battery" and "cell" may be used interchangeably.

Briefly described the present invention is directed at a circuit that provides a power regulation loop that operates in two modes and uses a single  
5 comparator. One mode, an open mode, involves generating an overload signal when the pass transistor is in an oversaturated mode indicating that the voltage drop of the device exceeds a predetermined threshold. The other mode, a linear mode, involves generating an optimal value sense resistor for a liner mode operation of a pass transistor. The two modes do not exist simultaneously and, therefore, a single comparator may be used  
10 between the two modes.

FIGURE 1 shows a circuit for a power regulation loop that operates in two modes using a single comparator, in accordance with aspects of the invention. As shown in the figure, power regulation loop 100 includes a power supply, resistors  $R_S$ ,  $R_X$  and a LOAD, transistor Q1, transistor M3, amplifier circuit 125, comparator 135,  
15 mode circuit 130, control 140, and switch 150.

Transistor Q1 has an emitter coupled to the power supply, a base coupled to ground, and a collector coupled to node N110. Transistor M3's source and drain are coupled between node N125 and node N130. Resistor  $R_S$  is coupled between node N130 and ground. Amplifier circuit 125 has an input coupled to node N110, an input  
20 coupled to node N125, and an output coupled to the gate of transistor M3. Mode circuit 130 has an input coupled to node N120 and an output coupled to an input of comparator 135. The load (LOAD) is coupled between node N110 and ground. Control 140 has an input coupled to node N140, an input coupled to node N145 and an output coupled to node N120.

25 The operation of power regulation loop 100 will now be described. The circuit illustrated in FIGURE 1 illustrates PNP transistor Q1 operating in full open mode. The circuit may operate in two modes including an open mode and a linear control mode. During operation in full open mode, the regulation circuit (Q1) acts as a full open switch. During operation in the open mode, the power regulation loop utilizes  
30 comparator 135 to determine when PNP Q1 goes into a saturation overload condition.

The power supply provides power to transistor Q1. The base of Q1 is shown coupled to ground indicating that Q1 is in full open mode. Typically as long as the current passing through transistor Q1 is less than a current regulation limit, the transistor is run in full open mode.

5                    Amplifier 125 is arranged to control transistor M3. Generally, amplifier 125 operates to keep its input terminals at the same voltage that are coupled to the emitter (E) and collector (C) of PNP Q1. Resistor  $R_S$  is used to generate a voltage that is proportional (e.g. gain scaled or attenuated) to  $V_{CE}$  across transistor Q1.

When the signal at node N130 ( $\approx V_{CE} \frac{R_s}{R_x}$ ) is greater than a

10    predetermined mode signal output by mode circuit 130, comparator 135 trips causing switch 150 to activate. The mode signal corresponds to a signal that has been predetermined to correspond to a saturation overload associated with transistor Q1. When comparator 135 detects an overload, switch 150 is coupled to linear control mode node N140 and the power regulation loop switches to a linear mode (See FIGURE 2).

15                    FIGURE 2 illustrates a circuit for a power regulation loop arranged to operate in linear mode, in accordance with aspects of the invention. The circuit illustrated in FIGURE 2 is substantially the same as illustrated in FIGURE 1 except that switch 150 now couples comparator 135 to a linear mode control node N140 instead of the open mode control node N145. Mode circuit 130 has also been expanded to show  
20    resistor ladder  $R_{1-3}$ , and MUX 230. Controller 245 is also shown.

MUX 230 has an input coupled to bus N120 and an output coupled to an input of comparator 135. Resistors  $R_{1-3}$  form a resistor ladder coupled to a voltage reference  $V_{REF}$ . MUX 230 is coupled to four tap points. MUX 230 may be coupled to more or less tap points. For example, MUX 230 could be coupled to two tap points or  
25    N tap points. Controller 245 has an input coupled to bus N120 and an output coupled to the base of transistor Q1.

The operation of FIGURE 2 will now be described. When the switch is coupled to node linear control node N140, the circuit operates pass transistor Q1 in a linear current control mode and regulates the current to the load. For example, when

Q1 is operating in a linear current control mode a trickle charge could be applied to the load.

Controller 245 operates to regulate the current to the load. Controller 245 responds to a control signal sent from control 140 by allowing an appropriate  
5 amount of current to reach the load. In embodiments of the invention, controller 245 is as simple as an amplifier or as complicated as microprocessor. In other embodiments, control logic may be used to aid in determining the output of control 140.

Comparator 135 is selectively coupled to one of four tap points along the resistor ladder during operation of the circuit in linear mode. Control 140 outputs a  
10 control signal to select one of the tap points within the resistor ladder. The MUX is set to select the next tap point in the resistor ladder until  $V_{CE}$  equals the selected tap point as determined by comparator 135.

According to one embodiment, switch 150 is moved to full open mode after the circuit has operated in linear control mode for a predetermined amount of time.  
15 According to one embodiment, switch 150 couples comparator 135 to the open control mode (node N145) after one minute of operation in linear current control mode. Other time periods may be used to move operation of the circuit into full open mode. Additionally, other conditions may be used to switch into full open mode. For example, a temperature sensor may be used to trigger the switch.

20 As long as an overload condition is not detected and the predetermined time period has not expired, the circuit will stay in full open mode.

The use of a single comparator for the two different modes provides many advantages. One advantage is that there is only a single offset associated with the comparator for the two different modes. Another advantage is that a component is  
25 saved as there is only one comparator instead of two.

FIGURE 3 illustrates a process for a power regulation loop that operates in two modes using a single comparator, in accordance with aspects of the invention. After a start block, the circuit starts in open mode and the process moves to block 310 where  $V_{CE}$  is compared to an overload signal that represents when a regulation circuit is  
30 in a saturation overload condition. Flowing to decision block 320 a determination is

made as to when an overload condition exists. When an overload condition is not detected, the process returns to block 310 to continue monitoring. When an overload condition exists, the process moves to block 330 where the circuit switches to a linear current control mode. Flowing to block 340 the MUX is adjusted to select a tap point  
5 on a resistor ladder. According to one embodiment of the invention, four tap points are used. According to other embodiments, more or less tap points may be used depending on the desired resolution. The process then moves to block 350, where  $V_{CE}$  is compared to the signal at the selected tap point. The comparisons made in blocks 310 and 350 utilize the same comparator. Transitioning to decision block 360 a determination is  
10 made as to whether to switch to open mode. According to one embodiment of the invention, the determination to switch depends on a predetermined amount of time (e.g. one minute) spent in linear current control mode. As discussed above, other conditions may be used to determine when to switch to open mode. When it is not desired to switch to open mode, the process returns to block 340 and the MUX is set to select the  
15 next tap point in the resistor ladder. The MUX continues to select different tap points until  $V_{CE}$  equals the selected tap point. When it is desired to switch to open mode, the process transitions to block 370 where the circuit switches to open mode. The process then moves to an end block and returns to processing other actions.

The above specification, examples and data provide a complete  
20 description of the manufacture and use of the composition of the invention. Since many embodiments of the invention can be made without departing from the spirit and scope of the invention, the invention resides in the claims hereinafter appended.